ORTEC
INCORPORATED
AN EG&G COMPANY

Model 473A
Constant-Fraction
Discriminator
Operating and Service Manual

ORTEC 473A CONSTANT-FRACTION DISCRIMINATOR

Manual Change Sheet

January 10, 1977

On schematic 473A-0201-S1, at the back of the manual, two sections of the 4-position mode selector switch have been labelled incorrectly. They are near the lower left corner of the schematic. Change the indicated sections, marked S1C and S1D, to identify these as S2C and S2D.

Model 473A
Constant-Fraction
Discriminator
Operating and Service Manual

This manual applies to instruments marked
"Rev 06" on rear panel

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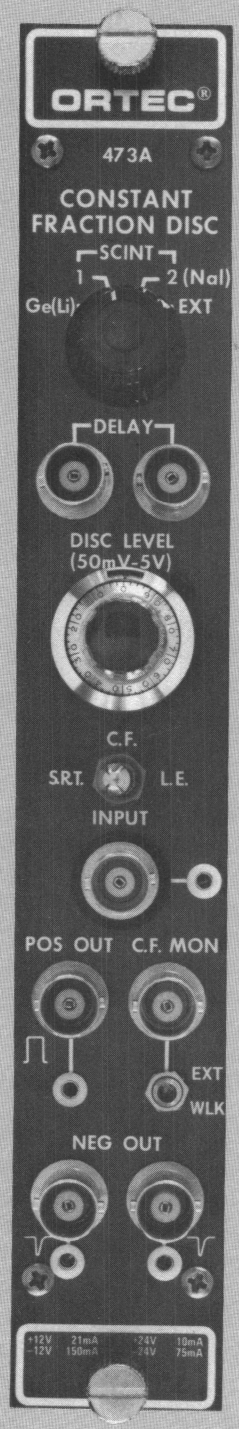

ORTEC®
473A
CONSTANT
FRACTION DISC
SCINT
1
2 (NaI)
Ge(Li)
EXT
DELAY
DISC LEVEL
(50mV-5V)
C.F.
S.R.T.
L.E.
INPUT
POS OUT
C.F. MON
EXT
WLK
NEG OUT
+12V
-12V
21mA
150mA
-24V
24V
10mA
75mA

ORTEC 473A Constant-Fraction Discriminator

1. GENERAL

1.1. FUNCTIONAL DESCRIPTION

The ORTEC 473A Constant-Fraction Discriminator provides logic signals that are used for precise timing measurements. The outputs are derived from input pulses that originate in almost any style of nuclear detector. The Constant-Fraction technique used to obtain the timing signals ensures accuracy and precision through a wide dynamic range of input signal amplitudes.

Shaping details are selected with front panel controls. A shaping selector switch is marked Ge(Li), Scint 1, Scint 2 (NaI), and Ext. These settings select circuits that are most appropriate to a variety of detector types or a circuit that can be controlled externally to normalize operating characteristics for other applications.

The Scint 1 setting is intended for detector systems having very fast rise-time signals such as those obtained with very fast photomultiplier tubes. The Scint 2 (NaI) setting is appropriate for many detectors having fast rise-time signals such as those obtained from fast scintillators and fast photomultiplier tubes. Also, the Scint 2 (NaI) setting is appropriate for most NaI(Tl) type detectors, as implied by the marking NaI. Since the switch selections differ only in the delay time, t_d, used for the Constant-Fraction technique, the indicated detector types are general classifications rather than being strict selection criteria. The specific characteristics of each type of detector can differ through a wide range and cannot be served by any unique delay time. But the 473A, including its Ext selection, can be used to optimize the operation experimentally for any specific detector.

When the collection times in the detector, and therefore the rise times of its output pulses, vary through a wide time range, it is often advantageous to connect the detector's preamplifier output through an ORTEC 454 Timing Filter Amplifier before it reaches the input to the 473A. The 454 can also be used to amplify preamplifier output signals if they do not have sufficient amplitudes to drive the 473A with the signals that represent energies of interest. When a minimum rise time is particularly important, the ORTEC AN302/N Fast Quad Amplifier can be used to advantage.

In addition to the basic Constant-Fraction timing signal derivation, the 473A permits selection of a S.R.T. (slow rise-time signal reject) operating mode so that an input signal with a rise time that is too slow to provide accurate timing information will be rejected. When this variation from the basic Constant-Fraction mode is selected, each input signal with a rise time greater than about 25 ns, measured between the C.F. pickoff-discriminator level and the front panel adjusted Disc Level, will not generate an output. The C.F. pickoff-discriminator level is automatically adjusted to 50% of the front panel adjusted Disc-Level setting. Although signal rejection reduces the efficiency of operation, the timing resolution of the remaining output signals is improved by using this mode when there are signals with slow rise times.

The mode selector switch also includes a setting for L.E. (Leading-Edge) discriminator operation. In this mode the Constant-Fraction circuitry is bypassed and the unit operates as a conventional leading-edge discriminator. The shaping selector switch at the top of the front panel has no effect during L.E. operation except that the input count rate is limited to about 1 MHz if the switch is set at Scint 2 (NaI); otherwise the count rate limit is about 15 MHz.

The adjustments and selections are usually quite simple. Just select the appropriate detector identification, set the Disc Level for the lowest energy of interest, select the desired mode of operation, and connect the input and output cables. The 473A then provides the timing signals with excellent precision and stability, suitable for even the most sophisticated time-spectroscopy measurements.

For convenience, monitor test points are included for inspection of input and output signals and for the Constant-Fraction walk adjust effects. The appropriate delay and attenuation conditions are selected according to the type of detector. The maximum benefits of using the Constant-Fraction technique are obtained without any unnecessary calculations. But there is also a provision for external control, to permit experimentation or to provide for those unusual conditions that require delays or fractions other than the standard values that are switch-selected.

Although the switch selections do not include surface-barrier detectors, the 473A serves this class of detectors equally for time derivation signals. There are two general types of surface-barrier detectors; one includes a shaping preamplifier such as the ORTEC 140 Detector-Preamplifier Timing System, and the other provides a long time-constant decay for the preamplifier output signals. The proper setting for the 473A selector switch depends on both the input signal shape and the dynamic range. Often, for a fast rise-time input signal having a narrow dynamic range, the optimum 473A setting is the Ge(Li) mode since this provides true Constant-Fraction timing. When the input signal has a wide dynamic range, the Scint 1 or Scint

2 (NaI) setting may give the best results. In general, if the input to the 473A is taken from an ORTEC 454 Timing Filter Amplifier, the optimum 473A switch setting is the Ge(Li) position. When the 473A input is taken from an AN302/N Quad Amplifier, the best operation with the 473A depends on the input signal rise time and dynamic range and may be provided by either the Ge(Li) or Scint 2 (NaI) setting. In special cases, the Ext setting can be used and a user-selected delay cable can provide the optimum performance.

1.2. PHYSICAL DESCRIPTION

The 473A is a NIM-standard single-width module that must be installed in a bin and power supply for operation. All of the normally-used connections and controls are located on the front panel.

The required operating power will be furnished from the bin and power supply into which the module is installed for operation.

2. SPECIFICATIONS

2.1. PERFORMANCE

INPUT PULSE CHARACTERISTICS Negative pulses accepted to 5 V without saturation; protected to 100 V for duty cycle of 10%.

DISCRIMINATOR RANGE −50 mV to −5 V.

WALK AND DYNAMIC RANGE
Ge(Li) Mode ≤±2 ns for range of 100 mV to 5 V with 40-ns rise time.
Scint 1 Mode <±200 ps for range of 50 mV to 5 V (including test attenuator walk) with 1-ns rise time.
Scint 2 (NaI) Mode <±500 ps for range of 50 mV to 5 V with 5-ns rise time.

NOMINAL PULSE PAIR RESOLUTION For input signals >0.5 V with rise time <2 ns.
Ge(Li), Scint 1, or Ext 65 ns.
Scint 2 (NaI) 1.1 μs.

TEMPERATURE CHARACTERISTICS
Disc Level Drift typically ≤0.5 mV/°C, 0 to 50°C.
Propagation Delay Stability typically within ≤15 ps/°C, 10 to 40°C.

2.2. CONTROLS

SHAPING MODE 4-position front panel switch:
Ge(Li), Scint 1, Scint 2 (NaI) Select the delay and fraction for optimum time resolution for signals according to general detector-type classifications. The Scint 2 (NaI) setting also selects an internal dead time of ~1 μs to prevent multiple triggering on slow-decay signals.
Ext Allows selection of whatever delay is desired by controlling the length of coaxial cable attached between front panel connectors; also allows an internal jumper selection of 10%, 20%, or 30% for the triggering fraction (factory set for 30%).

TIMING MODE 3-position front panel switch selects time derivation mode:
C.F. Constant-Fraction timing operation; triggering fraction and shaping delay controlled by the shaping mode selection.
S.R.T. Rejects slow rise-time detector pulses; less efficient than the C.F. mode but provides better time resolution in many applications. Any signal that does not cross the input Disc Level within ~20 ns after the response at the constant-fraction pickoff level (50% of Disc Level) will not generate an output. Ideal for improving time resolution when using large Ge(Li) detectors.
L.E. Bypasses constant-fraction circuitry, allowing operation as a leading-edge discriminator whose count rate is limited by the dead time associated with the shaping mode selectors. Maximum count rate limited to about 1 MHz for Scint 2 (NaI); operates to 15 MHz for other selections.

DISC LEVEL 10-turn precision locking potentiometer adjusts the trigger level of the signal input discriminator; range, −50 mV to −5 V. Also adjusts the threshold level for an internal constant-fraction pickoff arming discriminator level.

EXT WLK 20-turn screwdriver adjustment for precise setting of walk compensation for External mode operation.

2.3. INPUT

NEG Front panel BNC accepts negative input signals from a fast preamplifier such as the ORTEC 9301, a fast amplifier such as the AN302/N or 574, or a shaping amplifier such as the 454; normal range from Disc Level to −5 V; input impedance, 50Ω. Reflections typically <10% for input signals to −5 V with rise time ≥1 ns. Input directly compatible with current pulses from PM anodes.

2.4. OUTPUTS

NEG Two NIM-standard fast-negative logic output signals generated separately and furnished through two BNC connectors on front panel; nominally −16 mA (800 mV on 50Ω load); width, ≤10 ns; rise time, ≤2.5 ns.

POS NIM-standard slow-positive logic output signal furnished through BNC connector on front panel; nominally +5 V, width, 500 ns; rise time, ≤25 ns; output impedance, ≤10Ω.

C.F. MON Permits observation of the Constant-Fraction shaped signal through BNC connector on front panel; output impedance, 50Ω.

2.5. EXTERNAL DELAY

DELAY Front panel input and output connectors for selecting the required shaping delay by controlling the length of 50Ω cable added between these BNCs; used for Ext mode operation only.

2.6. ELECTRICAL AND MECHANICAL

POWER REQUIRED +12 V, 21 mA; −12 V, 150 mA; +24 V, 10 mA; −24 V, 75 mA; 115 V ac, 42 mA.

DIMENSIONS NIM-standard single-width module (1.35 by 8.714 in.) per TID-20893.

3. INSTALLATION

3.1. GENERAL

The 473A is used in conjunction with an ORTEC 401/402 Series Bin and Power Supply, which is intended for rack mounting. Therefore if vacuum tube equipment is operated in the same rack, there must be sufficient cooling with circulating air to prevent any localized heating of the all-transistorized circuitry used throughout the 473A. The temperature of equipment mounted in racks can easily exceed the recommended maximum limit of 120° F (50° C) unless these precautions are taken.

3.2. CONNECTION TO POWER

Always turn off power for the power supply before inserting or removing modules. The ORTEC modular instruments are designed so that it is not possible to overload the power supply with even a full complement of modules in the bin. Since, however, this may not be true if the bin contains modules other than those of ORTEC design, use the convenient test points on the front panel of the 401/402 to check each power supply voltage level after all modules are inserted.

3.3. INPUT CONNECTION

The input circuit of the 473A is designed for use with a 50Ω cable. The input impedance is 50Ω, so no external terminator is required for this connection.

The input can come from a detector or photomultiplier directly, provided it has negative polarity and the pulse amplitudes for the energies of interest will exceed a Disc-Level setting in the 473A. When the input signal has a fast rise time (0.5 to 5 ns) and must be amplified, an ORTEC AN302/N Quad Amplifier can be used between the preamplifier output and the input of the 473A. When an amplitude requires both amplification and additional pulse shaping (such as with germanium detectors), an ORTEC 454 Timing Filter Amplifier can be used to furnish both of these functions between the output of the preamplifier and the input of the 473A.

3.4. OUTPUT CONNECTIONS

There are four outputs on the 473A, and all connectors are located on the front panel. Two of these are NIM-standard fast-negative logic pulses that are generated separately and are therefore completely isolated. A third is a NIM-standard slow positive pulse. All three logic pulses are furnished for each input pulse that exceeds the Disc Level unless the front panel switch selects S.R.T. and the rise time of the pulse is too slow. The fourth output is the C.F. Mon, which permits observation of the Constant-Fraction shaped signal.

The fast-negative output pulses are intended for timing applications such as the Start and Stop inputs to a time to pulse height converter. Either or both may be used and the alternate connector does not need to be terminated when not in use. Since the NIM-standard fast-negative pulse is a current pulse, and since it is intended for use with a 50Ω load, 50Ω cable should be used to connect it to the point where it will be used, and that point must be terminated in 50Ω. Normally the instrument that receives the pulse will have a 50Ω input impedance; if it does not, use an external termination at the output end of the cable.

The NIM-standard slow-positive output pulses can be used for coincidence work or can be counted directly in a scaler or ratemeter. It is normal to use 93Ω cable to transfer this voltage pulse; it is furnished through an output impedance of ≤10Ω. For cable lengths of more than 2 meters (~7 ft) it is recommended that the cable be

terminated in its characteristic impedance. This output can also drive a terminated 50Ω cable, but with a slightly reduced amplitude.

3.5. EXTERNAL CONTROL

If the optional external control is selected in lieu of one of the identified detector types, the Constant-Fraction circuit is not complete until the two front panel Delay connectors are cabled. If they are directly shorted, the delay is zero. For a calculated delay, use a length of RG-174 50Ω cable for the connection. The adjusted delay is a function of cable length, based on 125 ps/inch of this type of cable.

The factory-installed connection to select the fraction for Ext operation uses the circuit for a 30% triggering fraction. By moving a jumper on the printed circuit board, the triggering fraction can be changed to 10% or 20% if desired for experimental work.

4. OPERATION

After the 473A has been installed and interconnected as described in Section 3, the only operating functions that are normally required are the setting of the shaping selector switch, adjusting of the Disc Level control, and selecting the desired operating mode.

Normally the shaping selector switch can be set at a switch position that identifies the type of detector being used. However, the only differences between the three switch positions marked for detector types are the effective delay time that will be used for Constant-Fraction pickoff and the controlled dead-time duration in the output circuit. For reference, the selectable delay times are 14 ns for Ge(Li), 1.3 ns for Scint 1, and 1.9 ns for Scint 2 (NaI). Shaping that is provided by the preamplifier may affect the relation between the optimum switch selection and the actual class of detector that is being used. The output circuit dead time is nominally 65 ns when the shaping switch selects Ge(Li), Scint 1, or Ext. When the switch selects Scint 2 (NaI), the internal dead time is increased to 1 μs. If the switch is set at Ext, the delay time is determined directly by the length of 50Ω cable that is connected between the Delay BNC connectors on the front panel. Two additional functions are selectable when the switch selects Ext. One is the triggering fraction; the basic setting of a jumper on the printed circuit selects 30%, but the jumper can be moved to select 20% or 10% if desired. The other function is the front panel Ext Wlk control, and its setting can be optimized for each application of the Ext switch selection.

The purpose of the Disc Level adjustment is to accept signals with amplitudes of interest and to eliminate response to signals with smaller amplitudes. The proper setting of this control depends on the range of signal amplitudes that are furnished to the input. The control range is 50 mV to 5 V, using the 10-turn precision potentiometer for precise adjustment and excellent repeatability.

For most applications, the mode selector can be set at C.F., for Constant-Fraction operation. If the signal rise times tend to vary through a wide range, such as the signals that can be furnished from a large-volume coaxial germanium detector, the switch can be turned to S.R.T. to operate as a Constant-Fraction discriminator but to also reject each input pulse that has too slow a rise time. The S.R.T. selection then provides a better resolution in the timing spectrum.

Conventional leading-edge timing can be obtained with the mode switch set at L.E. If the shaping selector switch is set at Scint 2 (NaI), the internal dead time is held at 1.1 μs so the maximum input count rate is limited to just under 1 MHz. But if the switch selects any of the other three shaping circuits, the dead time is only 65 ns and the input count rate can be up to about 15 MHz maximum. The other functions selected by the shaping selector switch have no effect during Leading-Edge operation because the Constant-Fraction portion of the 473A circuits is bypassed.

5. THEORY OF OPERATION

5.1. GENERAL

The circuits of the 473A are shown in schematic 473A-0201-S1, included at the back of the manual.

The inputs are furnished simultaneously to three internal circuits. One circuit is a lower-level leading edge (LLLE) discriminator that defines the onset of a signal of interest and arms internal logic circuits in the module. A second circuit is an upper-level leading edge (ULLE) discriminator; each input signal must exceed this level in order

that an output will be generated. The third circuit is a constant-fraction (C.F.) discriminator that provides a precise timing recognition for each input signal.

A front panel Disc-Level control effectively adjusts the response threshold for both the lower-level and upper-level discriminators. The nominal range for this control is 50 mV to 5 V, referred to the input pulse amplitude and associated with the ULLE response level. The LLLE threshold is adjusted automatically to about 50% of the ULLE so that it is triggered earlier on the leading edge of the input pulse.

When an output is generated it furnishes two independent NIM-standard fast-negative signals and one NIM-standard slow-positive signal. The leading edges of the three output signals are coincident. A feedback in the output trigger circuit ensures generation of only one set of output pulses for each input pulse.

The Constant-Fraction mode of operation can be used either with or without the slow-rise time reject feature. When the S.R.T. setting is selected with the front panel toggle switch, the C.F. timing signal is not generated if the rise time of an input pulse is too slow. The leading-edge (L.E.) mode of operation does not use any of the constant-fraction or slow-rise time reject functions, but generates an output when there is an input signal that crosses the ULLE threshold.

5.2. INPUT CIRCUIT

Signals are accepted through front panel BNC CN1. The input is protected against large amplitude signals by Q1, D1, and D2. Resistor R42 provides 50Ω termination for the input signals and divides the input amplitude by a factor of 2. The input signals can be monitored at TP1 on the front panel.

The signals are furnished through R45 to three circuits. Buffer Q5 furnishes the signal to the LLLE discriminator; buffer Q7 furnishes the signal to the ULLE discriminator; and DL14 and DL15 connect the signal into the CF discriminator.

5.3. LOWER-LEVEL DISCRIMINATOR

The signal through Q5 is furnished to pin 9 of IC2(6) and the signal amplitude is compared to a reference level at pin 10. When the level at pin 9 exceeds the reference level, IC2(6) changes state and generates a response called LLLE for lower-level leading edge. The LLLE signal is used to reset the internal logic and to arm a zero crossing discriminator in the constant-fraction circuit. The response remains high at IC2(6) and low at IC2(7) until the input signal level decays through the reference level.

The reference level at pin 10 of IC2(6) is furnished from the ULLE front panel adjustment through R43 and R73, and is about 50% of the upper-level threshold. A calibrated baseline is furnished from R160 and R65 through Q4. The calibration, on the printed circuit, is furnished by R65, LLLE Adj.

5.4. UPPER-LEVEL THRESHOLD

The signal through Q7 is furnished to pin 9 of IC4(6) and its amplitude is compared to a reference level at pin 10. Under quiescent conditions, the level at pin 9 is less negative than the level at pin 10. When the amplitude at pin 9 exceeds the level at pin 10, IC4(6) changes state and generates a response called ULLE for upper-level leading edge. If ULLE is generated, this permits an output signal to be generated if it satisfies the other criteria. The ULLE response remains high at IC4(6) and low at IC4(7) until the input signal decays back through the reference level.

The reference level at pin 10 is furnished from the R66, R67, R69 circuit through Q6. The range is calibrated by R66 for the front panel level control, R67. The effective range, referred to the input, is 50 mV through 5 V.

5.5. CONSTANT-FRACTION DISCRIMINATOR

Each input signal is applied to two parallel circuits that lead into the constant-fraction discriminator. One circuit, through DL15, delays the input pulse, and the other circuit, through DL14, attenuates the signal. The resulting signals are furnished into a limiting differential amplifier to generate the unique constant-fraction signal that can be examined at the C.F. Mon connector on the front panel.

Shaping selector switch S1 selects the delay for one path and the attenuation factor for the other path. S1B and D select one of four delay paths; for Ge(Li), the delay is DL1 and consists of 9 ft 4 in. of 50Ω cable for a time of 14 ns; Scint 1 uses DL2 for 1.3 ns; Scint 2 (NaI) uses DL3 for 1.9 ns. When the switch selects Ext, the amount of delay is determined exclusively by the amount of 50Ω cable that is connected externally between the two front panel Delay connectors.

Switch sections S1A and C select R7 and R14 for Ge(Li); R8 and R15 for Scint 1; R9 and R16 for Scint 2 (NaI); or R10 through R13 for Ext. Each setting except Ext provides a triggering fraction of 32%. The Ext setting uses jumper selections in a step attenuator to choose triggering fractions of 10%, 20%, or 30%; the jumper is set for 30% when the unit is shipped from the factory and can be changed to either of the alternate settings on the printed circuit board. The value of the fraction, calculated by resistance values, is always greater than the effective fraction, *f*, because of inherent circuit delays.

A differential amplifier, IC1(6), (3), and (14), accepts the two shaped signals through buffers Q2 and Q3. This circuit generates a bipolar signal with zero crossover when the delayed signal amplitude exceeds the prompt attenuated signal amplitude. Since both signals are the

result of the same input pulse, the actual peak amplitude, within a normal range, does not affect the relative time at which the crossover occurs. A zero-crossing discriminator is then used to generate the C.F. response timing signal.

The only portion of the input pulse that is used for Constant-Fraction time derivation is the rise time. Figure 5.1 shows how two pulses with different peak amplitudes will generate identical timing responses at IC1(14). The delayed signal is furnished to pin 10 of IC1 and the attenuated signal is furnished to pin 9. When the negative polarity at pin 10 exceeds the amplitude at pin 9, the polarity of the limiting differential amplifier switches and drives gate IC3(14) if it has been enabled by LLLE. The result is that the C.F. trigger response time is the same for any original pulse amplitude within the normal response range for the 473A. The pulse that is generated in the differential amplifier is also furnished to the front panel C.F. Mon BNC connector, where waveforms can be observed that are similar to those shown in Figs. 5.2 and 5.3. Figure 5.2 is the summed constant-fraction waveform with the input from a Ge(Li) detector, and Fig. 5.3 is the same information where the input is from a NaI(Tl) detector and the mode switch selects Scint 2 (NaI).

In Fig. 5.2(a), the time on the baseline is 20 ns/cm and the zero crossover is difficult to determine. When the time base is changed to 2 ns/cm, the critical portion of the waveform is spread out so that the zero crossover point can be seen easily, as in Fig. 5.2(b).

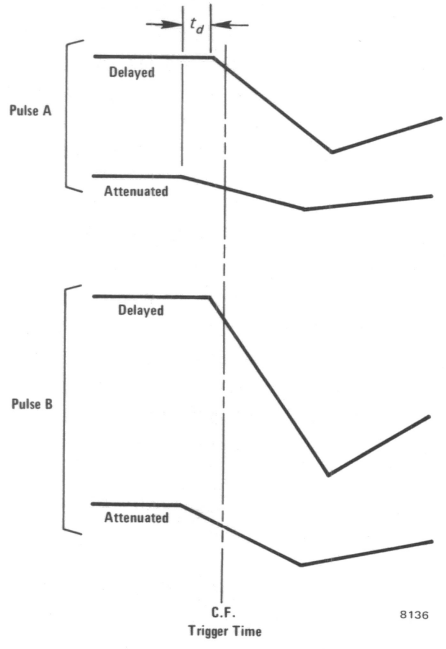
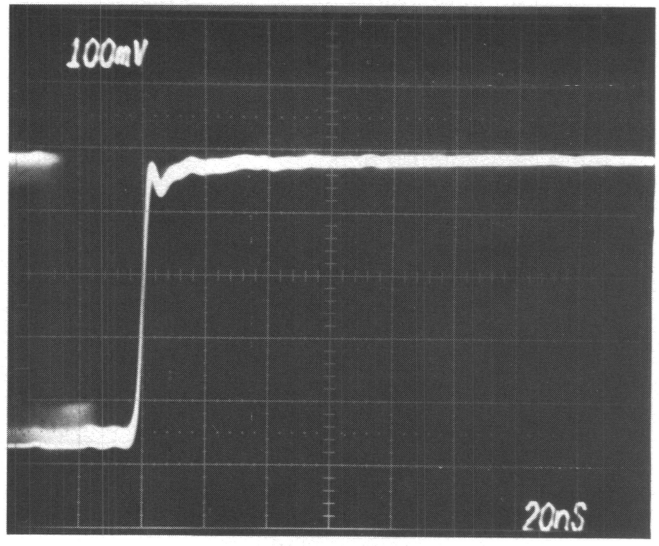
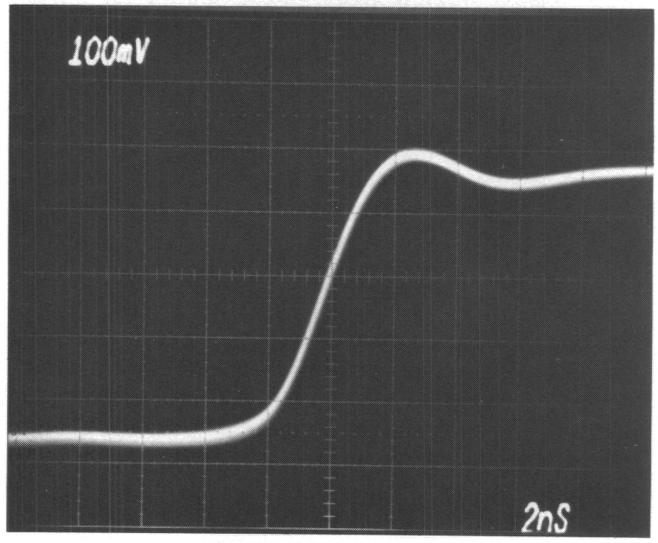


Fig. 5.1. Constant-Fraction Trigger Timing for Two Different Input Pulse Amplitudes.



(a) Display with 20 ns/cm



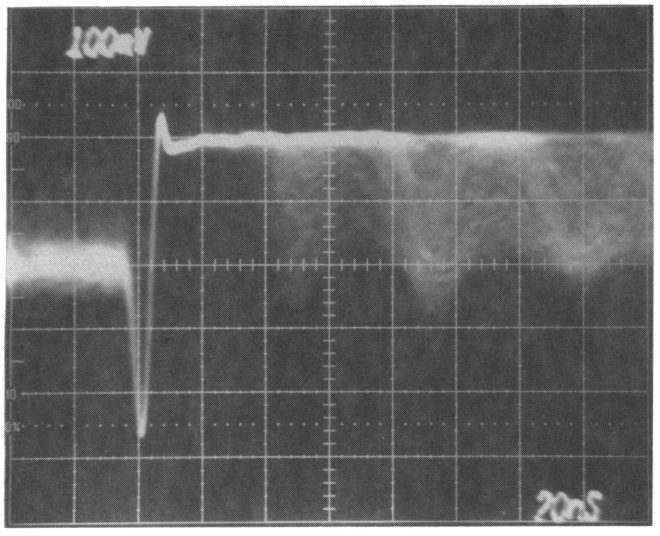
(b) Display with 2 ns/cm

Fig. 5.2. C.F. Mon Waveforms Using Ge(Li) Mode.

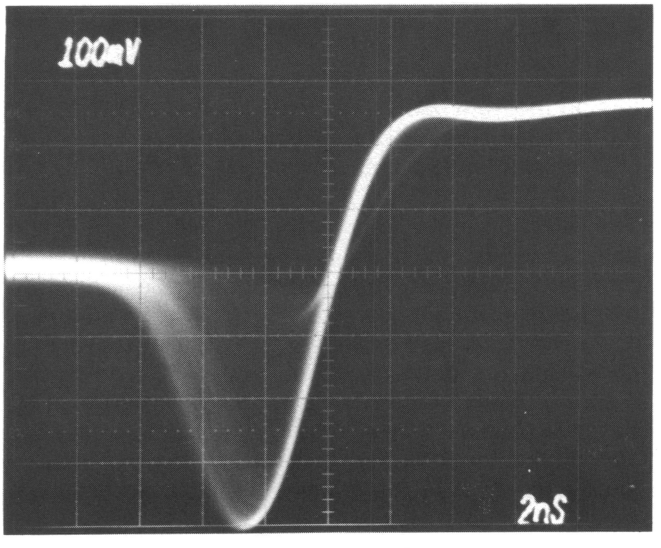
In Fig. 5.3(a), the time base of 20 ns/cm permits observation of some of the perturbations that may follow the scintillation detector waveform. These do not interfere in any way with the point of interest, which is the zero crossover that is shown clearly when the baseline is changed to 2 ns/cm as in Fig. 5.3(b).

Amplifier feedback is furnished through Q10, Q11, and through Q8, Q9. Potentiometer R35 is a walk adjust control on the printed circuit that sets the C.F. baseline to minimize time differences for all shaping modes; this adjustment is supplemented by the front panel Walk Adj control when shaping switch S1 selects Ext.

A timing pulse is generated at pin 12 of IC3(14) in response to a negative-going input variation at Input connector CN1 whether this is a real signal of interest or is



(*a*) Display with 20 ns/cm



(*b*) Display with 2 ns/cm

Fig. 5.3. C.F. Mon Waveforms Using Scint 2 (NaI) Mode.

simply a small amplitude pulse – generally noise – that is to be ignored. Gate IC3(14) will have been armed to pass the timing signal by LLLE if the signal is of interest.

5.6. CONSTANT-FRACTION OPERATION

Figure 5.4 is a simplified block diagram of the 473A that shows the relation of internal circuits when the C.F. mode of operation is being used.

Constant-Fraction timing discrimination provides a timing pulse for each input signal variation, whether this is converted into an output signal or not. The function described in Section 5.5 uses the CF stage (Fig. 5.4) to accomplish this signal generation. Note that the signal at signal used for time derivation. If the signal is of interest, it will have triggered the LLLE discriminator prior to the timing pulse, so gate G1 (in Fig. 5.4) is armed to pass the timing pulse.

After a delay of about 29 ns, during which other acceptance criteria are checked, the timing pulse is furnished to gate G2, which is IC3(7). A response in the ULLE circuit must have triggered flip-flop IC6(3) and (14) to indicate that the input signal amplitude is sufficient to satisfy the amplitude requirements, and the timing signal passes through G2 and G3 to trigger an output one-shot, IC10(7) and (14), to generate the group of three output signals.

5.7. S.R.T. OPERATION

Operation with the Slow Rise Time Reject circuit is the same as for the Constant-Fraction operation described in Section 5.6 except that the timing signal is blocked at gate G3 (Fig. 5.4) if the signal rise time is too slow. The S.R.T. (slow rise time) flip-flop, IC7(3) and (14), is reset by LLLE and is enabled, through IC8(15), to be set by flip-flop IC6(3) and (14). The S.R.T. flip-flop must have been set by the time the timing pulse reaches G3, IC9(6), or the timing pulse will not pass; the presumption is, then, that the rise time of the input pulse was too slow to qualify it as a true signal. The maximum rise time from LLLE to ULLE is about 25 ns to permit the output pulses to be generated.

5.8. LEADING-EDGE OPERATION

Conventional leading-edge discrimination can be selected by turning the mode selector switch to L.E. This enables IC8(2) and completes the signal path from ULLE to gate G2 (in Fig. 5.4) through the delay, DL9. The signal path starts at ULLE, where the input amplitude triggers a response when it exceeds the adjusted Disc-level setting. It is delayed while FF is triggered to enable G2, and then passes through G2, G3, and G4 to generate a set of three output signals and the dead-time feedback control.

The CF response is not effective because the G1-to-G2 path is not enabled. S.R.T. is set to enable G3 each time an FF response reaches its input in the L.E. mode, and it is reset from the trailing edge of LLLE. The FF continues to toggle between reset and set at LLLE and ULLE times, but it enables G2 each time there is a ULLE pulse coming through the delay line.

5.9. OUTPUT PULSE GENERATION

When a decision has been made to generate a set of output pulses, the signal is furnished to pin 5 of IC9(2). The signal passes through IC9(15) to trigger both NIM-standard fast-negative output pulse circuits and through IC9(14) to start Schmitt trigger IC10(7) and (14). The Schmitt trigger is the input to the NIM-standard slow-positive output generator.

One fast-negative output generator uses Q12 and Q13 as

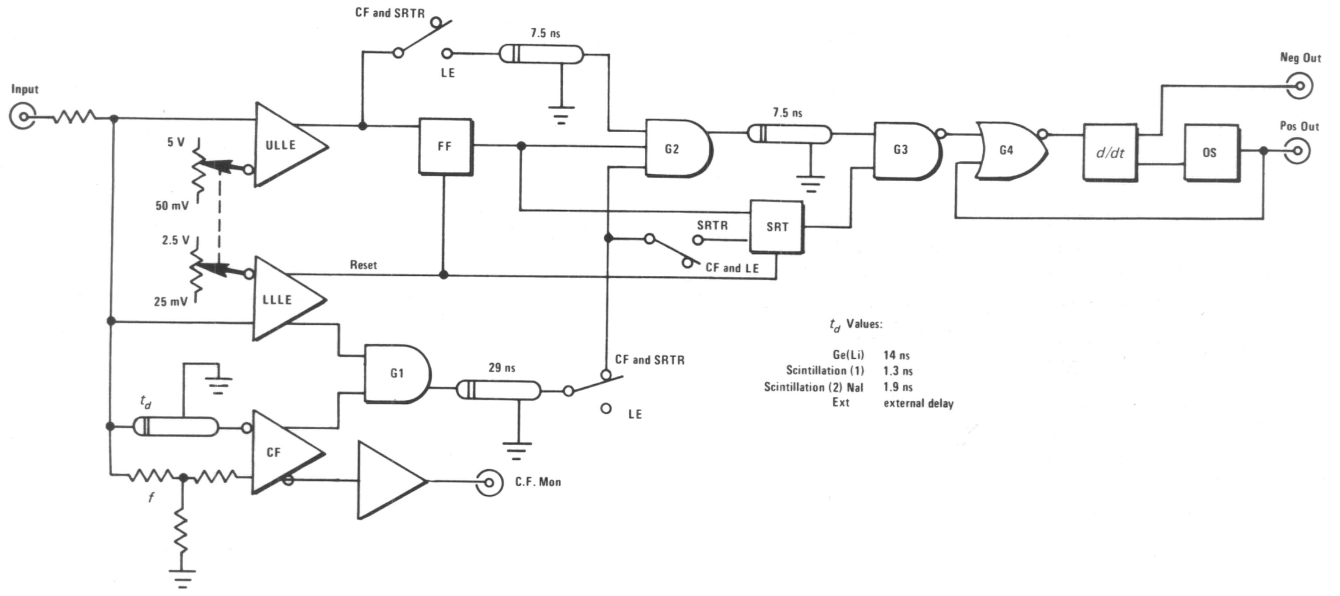


Fig. 5.4. Simplified Block Diagram of the 473A Constant-Fraction Discriminator.

normally flows through Q12. When the signal is furnished from IC9(15), Q12 is turned off and Q13 is turned on to furnish the current through CN2 on the front panel, assuming that the output current circuit is properly terminated in 50Ω. The other fast-negative output generator uses Q14 and Q15 as an identical current switch that is triggered by the same input signal from IC9(15) to switch −16 mA from Q14 to Q15 and through CN3 to the external circuit.

The Schmitt output at IC10(14) is furnished to the positive NIM one-shot circuit that includes Q16, Q17, and Q18. When the signal is furnished through C63 to Q16, the output at CN4 rises from 0 to a nominal +5 V for a period of about 500 ns.

The Schmitt output at IC10(14) is also coupled back to pin 4 of IC9(3) to hold this input high and prevent response to another input signal that arrives before a controlled dead time has elapsed. C55 is a stretch circuit that blocks the Schmitt circuit from recovering for a period that is determined by the setting of shaping switch S1. When switch S1 selects Ge(Li), Scint 1, or Ext, the recovery time of the Schmitt circuit is about 50 ns; but for the Scint 2 (NaI) setting of the switch, the recovery time is extended to about 1 μs.

5.10. EXTERNAL SELECTIONS

If the shaping selector switch is turned to Ext, three portions of the internal circuits shown in Fig. 5.3 are affected. The delay time and attenuation for CF operation and the trigger baseline level for the CF discriminator are all controllable.

The selection of delay, t_d, is dependent on the external circuit that is added between the two Delay BNC connectors on the front panel. If they are shorted directly, there is zero delay. Normally they will be connected with a measured length of 50Ω cable, with a delay of about 1.5 ns/ft.

The selection of the fraction for attenuation is a jumper connection at one of three alternate locations on the printed circuit board. They are located on the front corner of the printed circuit nearest switch S1 and are numbered 1, 2, and 3. A lead from the 2nd wafer of switch S1 completes the connection. Normally, the lead is connected to point 3 for a 30% dc fraction. The wire lead can be moved to point 2 for a 20% dc fraction or to point 1 for a 10% dc fraction if desired. The value of the dc fraction is always larger than the effective fraction, *f*, because of inherent circuit delays.

After the fraction setting has been completed, test the output signal timing for walk caused by input signal amplitude variations. The Walk Adj control on the front panel adjusts the reference level that is furnished to pin 9 of IC1(6) together with the attenuated input signal. It needs to be adjusted for each change of the fraction selected for Ext operation, and is not in the circuit for any of the alternate shaping modes.

The remaining portion of the Fig. 5.3 circuits that are affected by the selection of Ext is the duration of dead time, which is in the feedback loop from the Pos Out circuit to gate G4. Section E of switch S1 completes a circuit from the switch wiper to ground for the Ge(Li), Scint 1, and Ext settings, and the resulting controlled dead time is approximately 65 ns. If a longer dead time is desired for Ext operation, the grounded connection for the 4th switch position can be clipped and the dead time will then be about 1 μs, the same as for Scint 2 (NaI) operation.

5.11. POWER SUPPLIES

Two power supply levels are generated in the 473A for use in its integrated circuits. One level is −5.2 V and the other is −2 V.

The ac input power line is connected through the bin and power supply to each module location. It is accepted from this circuit into the primary of transformer T1 on the 473A chassis. The output of T1 is a full-wave rectified source for −5.2 V, required in most of the integrated circuits. The voltage source is rectified by D5, regulated by Q20 through Q23, and filtered by C81. The −12 V bin power dc source is used as a reference.

Another circuit uses the −12 V reference and reduces the −5.2 V level down to −2 V for other operating requirements. Q25 is the series pass transistor in this dropping circuit and Q24 furnishes the reference level from a bleeder in the −12 V source.

Each of the four standard dc levels (±12 V and ±24 V) is accepted from the bin and power supply through a filter network. These four filters involve L12 through L15 and C73 through C80.

6. APPLICATIONS

6.1. TIMING WITH FAST SCINTILLATORS

Figure 6.1 shows a typical system for timing with fast scintillation detectors such as Naton-136, Pilot B, KL236, NE-102, NE-111, NE-213, etc. A 473A Constant-Fraction Discriminator is used in each of the two input channels to the time to pulse height converter. Figure 6.2 is a typical timing spectrum that was obtained with this system.

A plot of time resolution versus dynamic range is shown in Fig. 6.3 for a system using RCA 8850 photomultiplier tubes. A similar plot, using RCA 8575 photomultiplier tubes is shown in Fig. 6.4. The output pulse from the RCA 8575 is slightly slower than that from the RCA 8850. Because of this rise time difference, the best timing resolution was obtained with the 473A in the Scint 1 mode when using the RCA 8850. When using the RCA 8575, the best timing resolution was obtained with the 473A set for the Scint 2 (NaI) mode.

Input signals to the 473A should have a peak amplitude of about 5 V for the Compton edge of the 511-keV gammas

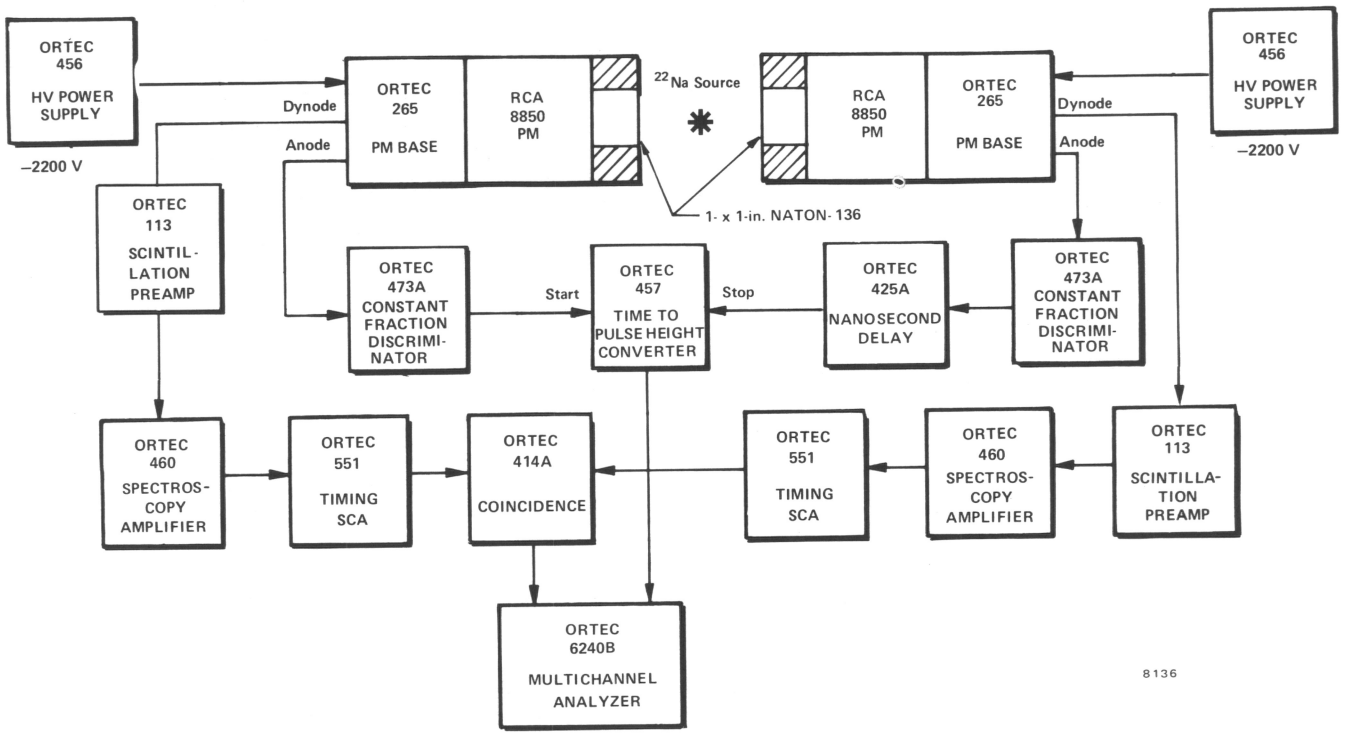
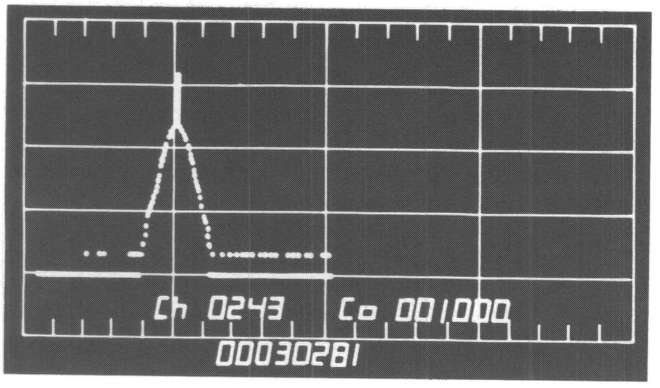


Fig. 6.1. A System for Gamma-Gamma Lifetime Measurement.



^{60}Co
RCA 8850 Photomultiplier Tube
1.1:1 Dynamic Range

FWHM 193 ps
FWTM 373 ps
6.85 ps per channel

Fig. 6.2. Timing Over a Narrow Dynamic Range with the System of Fig. 6.1.

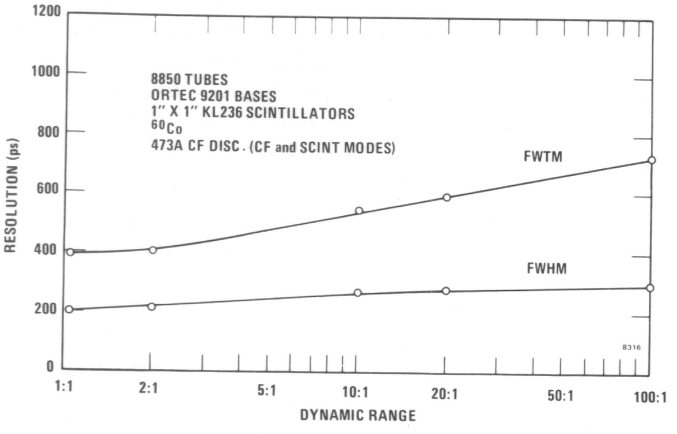


Fig. 6.3. Plot of Time Resolution vs Dynamic Range Using RCA 8850 Photomultiplier Tube.

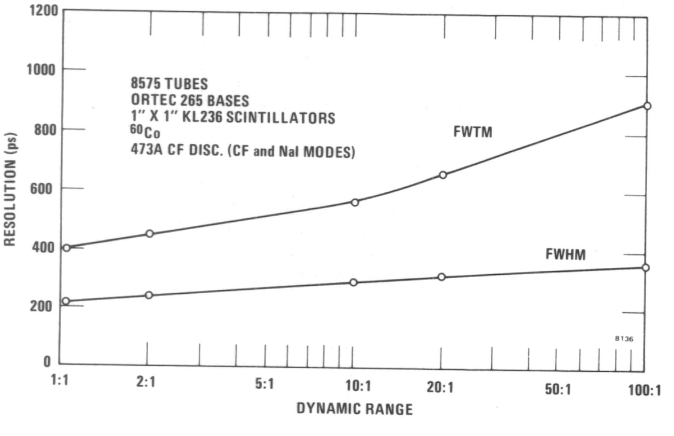


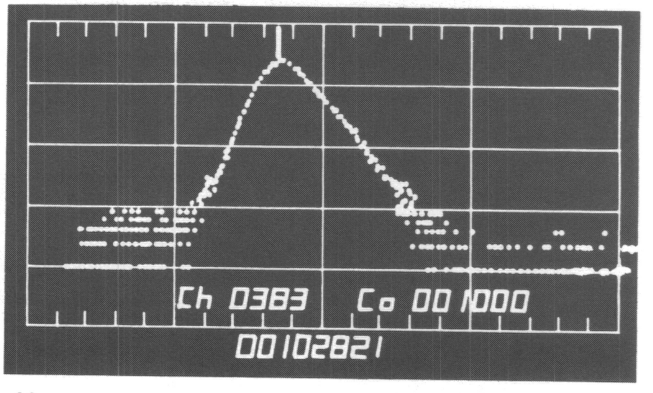
Fig. 6.4. Plot of Time Resolution vs Dynamic Range Using RCA 8575 Photomultiplier Tube.

from ^{60}Co so that a dynamic range of 100:1 can be achieved. The lower-level discriminator should be set at about 50 mV. For some tubes, the 50Ω termination that is internal to the tube base must be removed to accomplish the maximum dynamic range.

6.2. TIMING WITH NaI(Tl) SCINTILLATORS

This type of measurement is similar to timing measurements with fast scintillators. However, one additional problem must be considered. The photoelectron statistics for low-energy gamma-ray work are so poor that individual events near the trailing edge of NaI(Tl) pulses will trigger the 473A. Thus a single scintillation event can produce two or more discriminator output pulses. In the 473A, this problem is overcome by using the Scint 2 (NaI) mode, in which an internal dead time of about 1 μs is generated. The 473A can be used successfully on even longer-decay scintillators, but the internal dead time may have to be increased to prevent multiple triggering.

Figure 6.5 is a typical timing coincidence spectrum that was obtained with a NaI(Tl) detector and a KL236 fast plastic scintillator. Figure 6.6 is a plot of time resolution versus dynamic range for the timing system, with the NaI(Tl) detector mounted on an RCA 8575 PMT.



^{60}Co
Start: KL236 (1x1), RCA 8575 PMT
Stop: NaI (1x1), RCA 8575 PMT
50:1 Dynamic Range

FWHM 892 ps
FWTM 1.82 ns
9.7 ps per channel

Fig. 6.5. Typical Timing Spectrum Over a Wide Dynamic Range (50:1) with NaI(Tl).

6.3. TIMING WITH LARGE Ge(Li) DETECTORS

Figure 6.7 is a block diagram of another gamma-gamma coincidence system. In this system the start channel uses a fast scintillator and the stop channel employs a large coaxial Ge(Li) detector. A typical timing spectrum for a narrow dynamic range (1.1:1) is shown in Fig. 6.8 for both the C.F. and S.R.T. modes of operation. A similar spectrum for a wider dynamic range (10:1) is shown in Fig. 6.9. Note that the S.R.T. mode is more effective for timing with a wider dynamic range of signals. The S.R.T. mode can

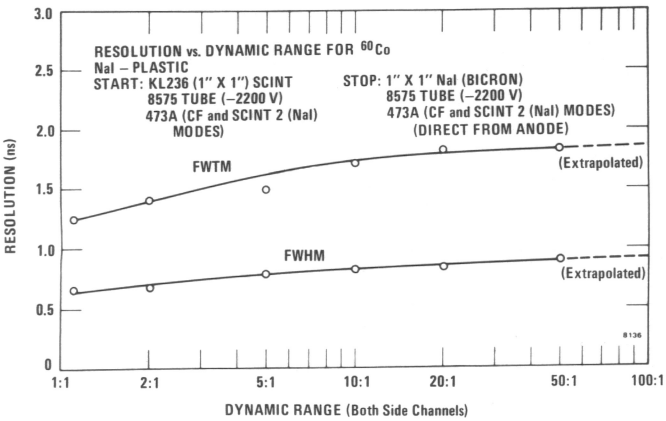


Fig. 6.6. Plot of Time Resolution vs Dynamic Range Using NaI(Tl) and RCA 8575 PMT.

provide dramatic improvements in timing resolution below FW(1/10)M and makes reliable timing data possible at even the FW(1/100)M level. Typical timing resolution data for various ORTEC Ge(Li) coaxial detectors are listed in Table 6.1.

The S.R.T. mode provides improved timing signals that result from input signals with excessively slow rise times.

Table 6.1. Timing Resolution for Various Sizes of Ge(Li) Coaxial Detectors Using ^{22}Na and the System of Fig. 6.7.

Detector	Dynamic Range	C.F. Mode		S.R.T. Mode		
		FWHM (ns)	FW(1/10)M (ns)	FWHM (ns)	FW(1/10)M (ns)	FW(1/100)M (ns)
8.6% 52.6 cc	1.1:1	4.4	10.1	4.3	10.1	21.6
	10:1	4.2	13.6	4.2	10.5	23.4
	20:1	4.7	13.5	4.7	12.8	30.4
VIP[10]	1.1:1	5.0	10.0	5.0	9.5	17.6
	10:1	4.5	13.2	4.4	9.4	17.8
	20:1	5.1	14.3	5.0	12.0	24.8
WIN[15]	1.1:1	7.9	16.4	8.1	16.0	27.3
	10:1	8.4	24.0	7.9	17.0	30.0
	20:1	8.4	26.0	8.4	23.0	40.0

Such input signals are generally associated with detector events in a weak field region. These events can represent valid energy data, and rejection of their respective timing signals corresponds to a reduction of detector efficiency. Since the 473A mode is front-panel-selectable, the experimenter can select either S.R.T. for the best timing resolution or C.F. for timing without loss of efficiency.

A plot of the percent loss of 511-keV peak counts from ^{22}Na for the S.R.T. mode, compared to the C.F. mode, is shown in Fig. 6.10 as a function of the 473A threshold and the detector size.

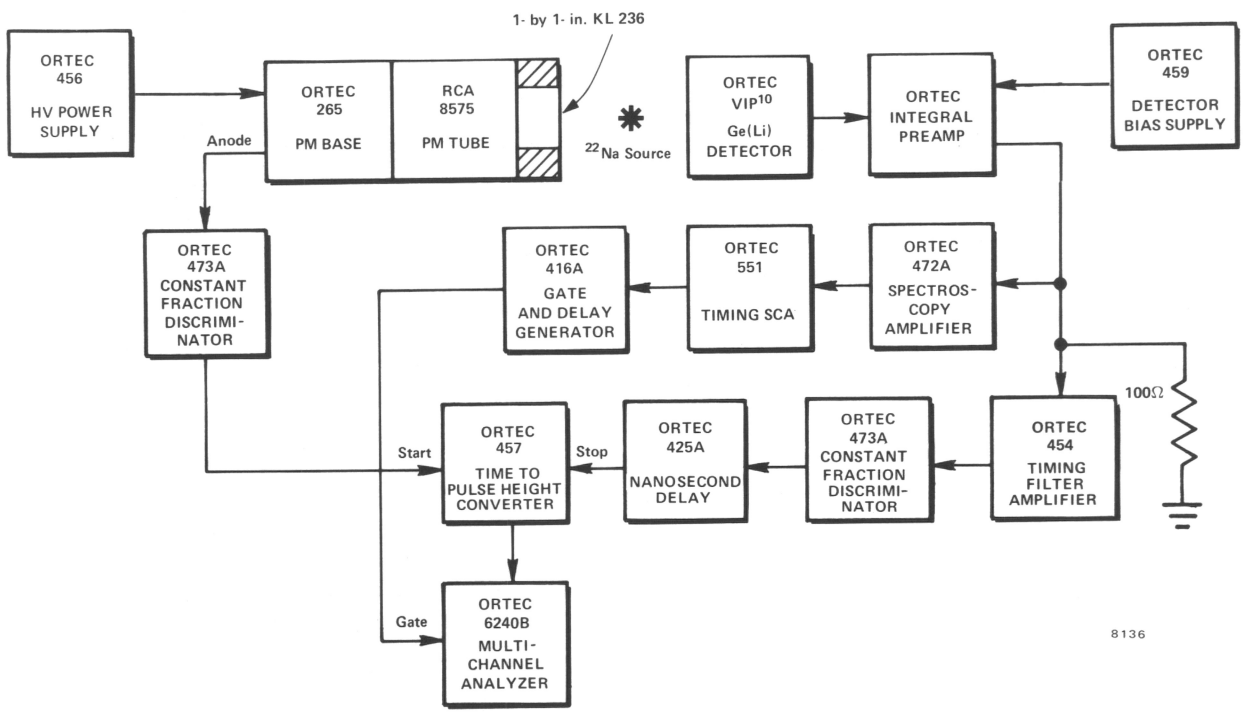
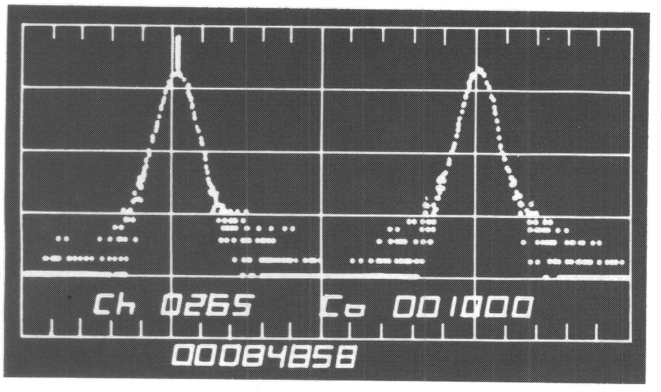


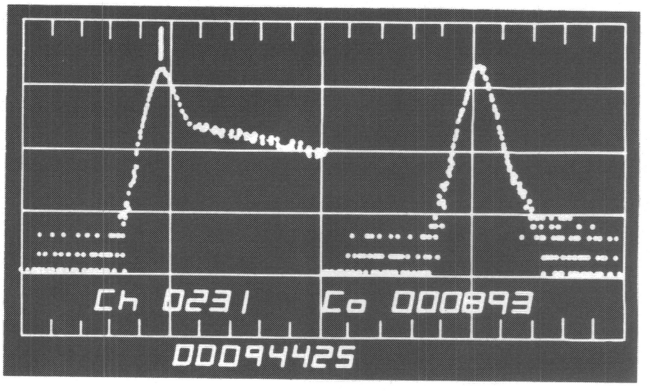
Fig. 6.7. Gamma-Gamma Coincidence System Using Plastic Scintillator and a Large Ge(Li) Coaxial Detector.



^{22}Na
Start: KL236 (1x1), RCA 8575 Photomultiplier Tube
Stop: Ge(Li) Coax, 12.5%, 62.3 cc
1.1:1 Dynamic Range

	CF	SRT
FWHM	5.0 ns	5.0 ns
FWTM	10.0 ns	9.5 ns
FW 1/100 M	17.2 ns	17.6 ns

Fig. 6.8. Timing Spectrum for a Narrow Dynamic Range (1.1:1) for the System of Fig. 6.7.



^{22}Na
Start: KL236 (1 x 1), RCA 8575 Photomultiplier Tube
Stop: Ge(Li) Coax, 12.5%, 62.3 cc
10:1 Dynamic Range

	CF	SRT
FWHM	4.5 ns	4.4 ns
FWTM	13.2 ns	9.4 ns
FW 1/100 M	–	17.3 ns

Fig. 6.9. Timing Spectrum for a Wide Dynamic Range (10:1) for the System of Fig. 6.7.

6.4. TIMING WITH OTHER DETECTORS

The 473A can be used to provide timing information from other detectors such as ORTEC surface-barrier detectors and low-energy photon detectors. When input signals are low-level and have very fast rise times, such as those from surface-barrier detectors, an ORTEC 574 Timing Amplifier is recommended as an accessory module.

ORTEC conducts a continuing program aimed at improved timing resolution. Please contact an ORTEC representative for information concerning any special requirements.

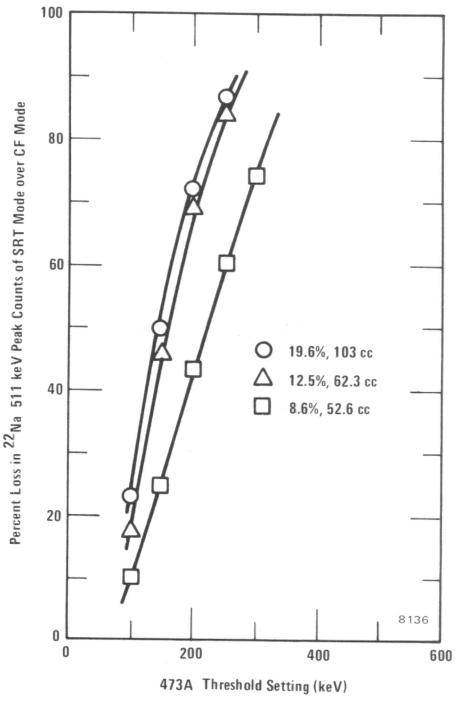


Fig. 6.10. The Effect of 473A Threshold Setting on the Apparent Efficiency of Different Ge(Li) Detectors.

7. CALIBRATION

7.1. EQUIPMENT REQUIRED

The following test equipment, or equal, is required to calibrate the 473A circuits:

1. ORTEC 401A/402A Bin and Power Supply
2. Hewlett-Packard 8004A Pulse Generator
3. Tektronix 485 Oscilloscope
4. Tektronix 10X Probe
5. Tektronix 50 Ohm Step Attenuator
6. Tektronix CT-3 Time Pickoff
7. EH 971-5 Rise Time Integrator
8. Fluke 8000A Digital Multimeter
9. ORTEC 425A Delay
10. ORTEC 457 Biased Time to Pulse Height Converter
11. ORTEC 448 Research Pulser
12. ORTEC 454 Timing Filter Amplifier
13. ORTEC 276 Photomultiplier Tube Base and Preamplifier

7.2. PRELIMINARY PROCEDURE

Install the 473A in the Bin and Power Supply and turn on the power. Allow the instrument to warm up for at least ten minutes before calibrating any of its circuits.

7.3. LEADING-EDGE DISCRIMINATOR TEST

1. Set up the system as shown in Fig. 7.1.

2. Monitor test point TP5 at the base of Q10 with a dc voltmeter. Adjust R32 as necessary to read −1.23 V at TP5.

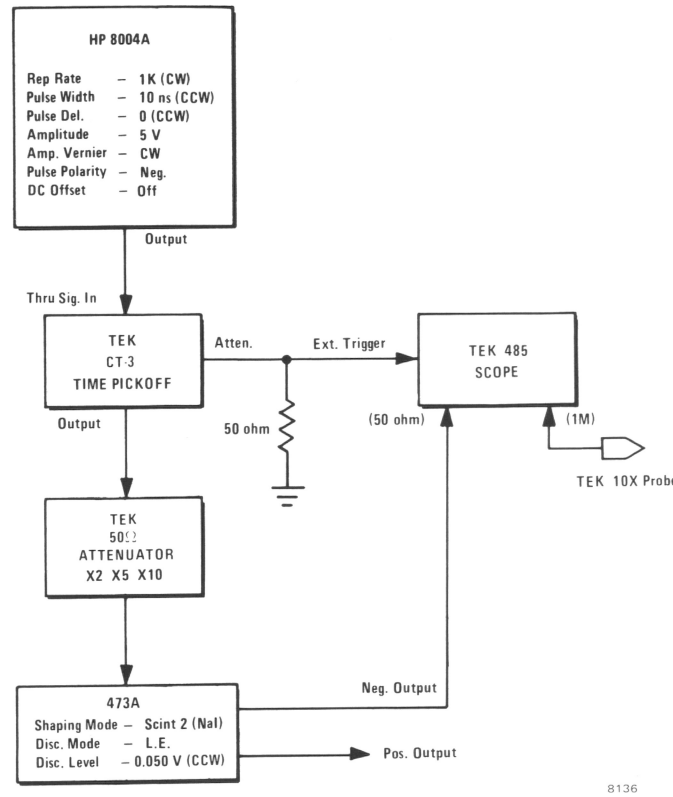
3. Turn front panel Disc Level control fully counterclockwise to its minimum reading of 50 dial divisions, for 50 mV.

4. Turn ULLE Adjust, R66, fully clockwise.

5. Monitor IC4(14) with the 10X oscilloscope probe.

6. Adjust R66 counterclockwise until the amplitude at IC4(14) is about 650 mV.

7. Turn HP8004A amplitude switch to 2.5 V.



NOTE: All cables are 50Ω coax (RG/58) unless otherwise specified.

Fig. 7.1. Test Setup for Leading-Edge Discriminator Mode Calibration.

8. Turn LLLE Adjust, R65, fully clockwise.

9. Monitor IC2(15) with the 10X oscilloscope probe.

10. Adjust R65 counterclockwise carefully until the signal at IC2(15) reaches about 800 mV.

11. Turn HP8004A amplitude switch to 5 V.

12. Monitor one of the negative output BNC connectors with the oscilloscope.

13. Adjust R66 carefully until the 473A output starts to appear.

14. Repeat steps 7 through 10.

7.4. SCINTILLATION 1 MODE WALK TEST

1. Set up the system as shown in Fig. 7.2.

2. Use X2X5 on the attenuator.

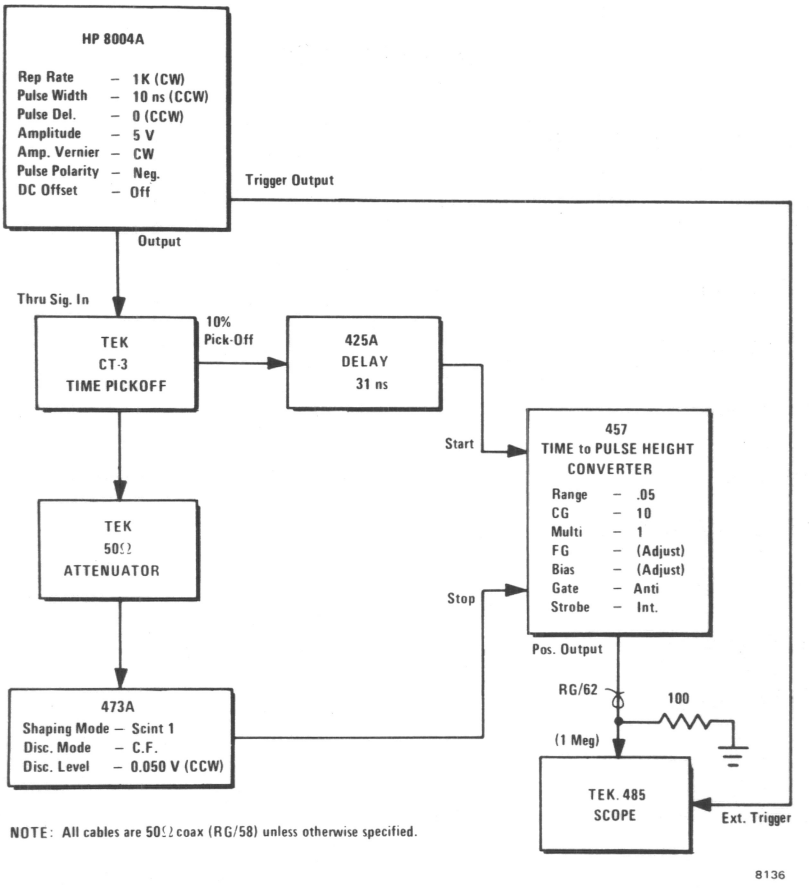


Fig. 7.2. Test Setup for Scintillation 1 Mode Walk Test.

3. Adjust the 457 Bias so that the 457 output pulse amplitude is about 5 V on the oscilloscope.

4. Set the vertical gain of the oscilloscope at 1 V per division.

5. Adjust the 457 Fine Gain and Bias controls until a change in delay of 1 ns corresponds to a 1-V (1-division) change in the 457 output.

6. Set the oscilloscope vertical gain at 0.2 V/division.

7. Adjust the 457 Fine Gain and Bias controls until a change in delay of 1 ns corresponds to a 5-division change in the 457 output; this calibrates the system for 200 ps/major division on the oscilloscope.

8. Change the attenuator in the following sequence while observing the oscilloscope: X5X10, X10, X1.

9. Adjust R32 as necessary so that the 457 output amplitude changes no more than 400 ps (2 divisions) for the attenuator changes in step 8.

10. Set the attenuator at X2X5X10 and observe the peak spread of the 457 output. If the spread exceeds 400 ps, adjust R32 to reduce it. Repeat steps 8 and 9. If R32 cannot be adjusted to satisfy both conditions, replace the MC10116 integrated circuit, IC1.

7.5. SCINTILLATION 2 (NaI) MODE WALK TEST

1. Set up the system as shown in Fig. 7.3. Adjust the HP 8004A output pulse width to 25 ns.

2. Use X2X5 on the attenuator.

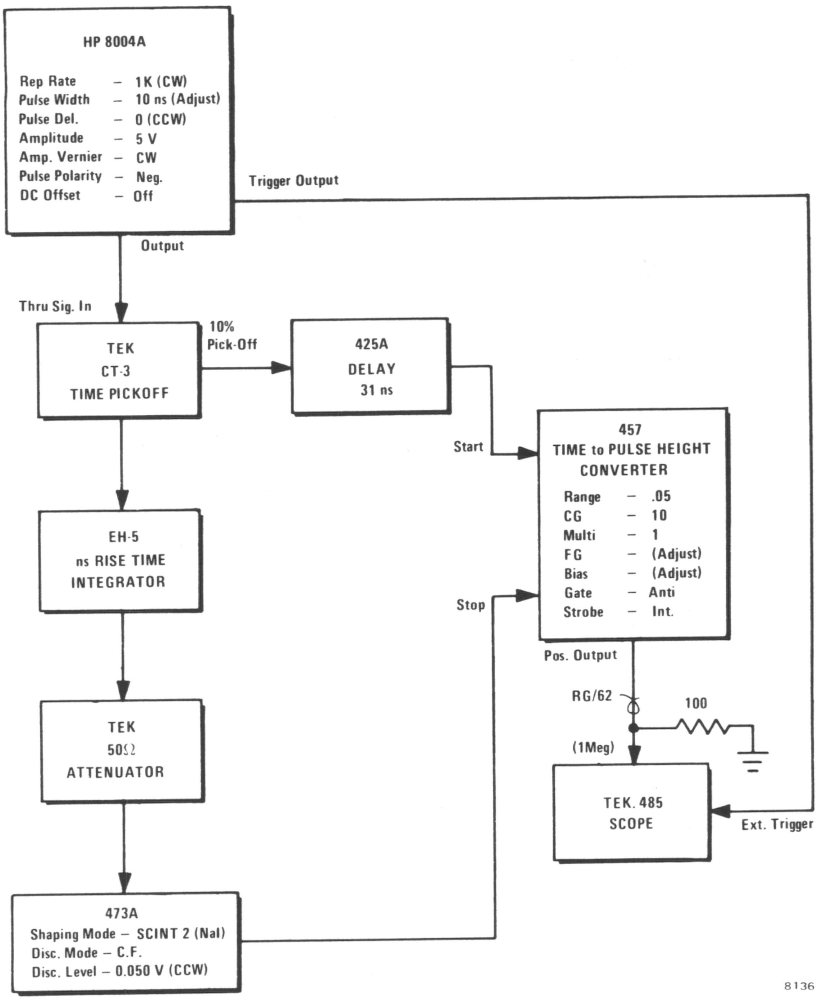
3. Adjust the 457 Bias so its output pulse shows about 6 V of amplitude as seen on the oscilloscope.

4. Set the vertical gain of the oscilloscope for 1 V per division.

5. Adjust the 457 Bias and Fine Gain until a change of 1 ns corresponds to a 1 V (1-division) change on the oscilloscope.

6. Change the oscilloscope vertical gain to 0.5 V per division.

7. Adjust the 457 Fine Gain and Bias until a 1-ns change corresponds to a change of 2 divisions on the oscillo-



NOTE: All cables are 50Ω coax (RG/58) unless otherwise specified.

Fig. 7.3. Test Setup for Scintillation 2 (NaI) Mode Walk Test.

scope. This calibrates the system for 500 ps/major oscilloscope division.

8. Change the attenuator in the following sequence while observing the oscilloscope: X5X10, X10, X1.

9. Adjust R32 as necessary so that the 457 output amplitude changes no more than 1000 ps (2 divisions) for the attenuator changes in step 8.

7.6. Ge(Li) MODE WALK TEST

1. Set up the system as shown in Fig. 7.4. With the attenuator set at X1, adjust the attenuator output for 5 V into 50Ω.

2. Set the attenuator at X2X5.

3. Adjust the 457 Bias so that the 457 output amplitude is about 5 V on the oscilloscope.

4. Set the vertical gain of the oscilloscope at 0.5 V/division.

5. Adjust the 457 Bias and Fine Gain until a change of 4 ns corresponds to a change of 1 V (2 divisions) on the oscilloscope. This calibrates the system so that one major division on the oscilloscope is equal to 2 ns.

6. Change the attenuator in the following sequence while observing the oscilloscope: X2X5, X5X10, X2X10, X10, X5, X1.

7. Adjust R32 as necessary so that the output amplitude from the 457 changes no more than 4 ns (2 divisions) for the attenuator changes in step 6.

8. If multipulsing occurs when the attenuator is set at X1 in step 6, turn the 473A front panel Disc-Level control to about 200 dial divisions, for 200 mV; the multipulsing should disappear.

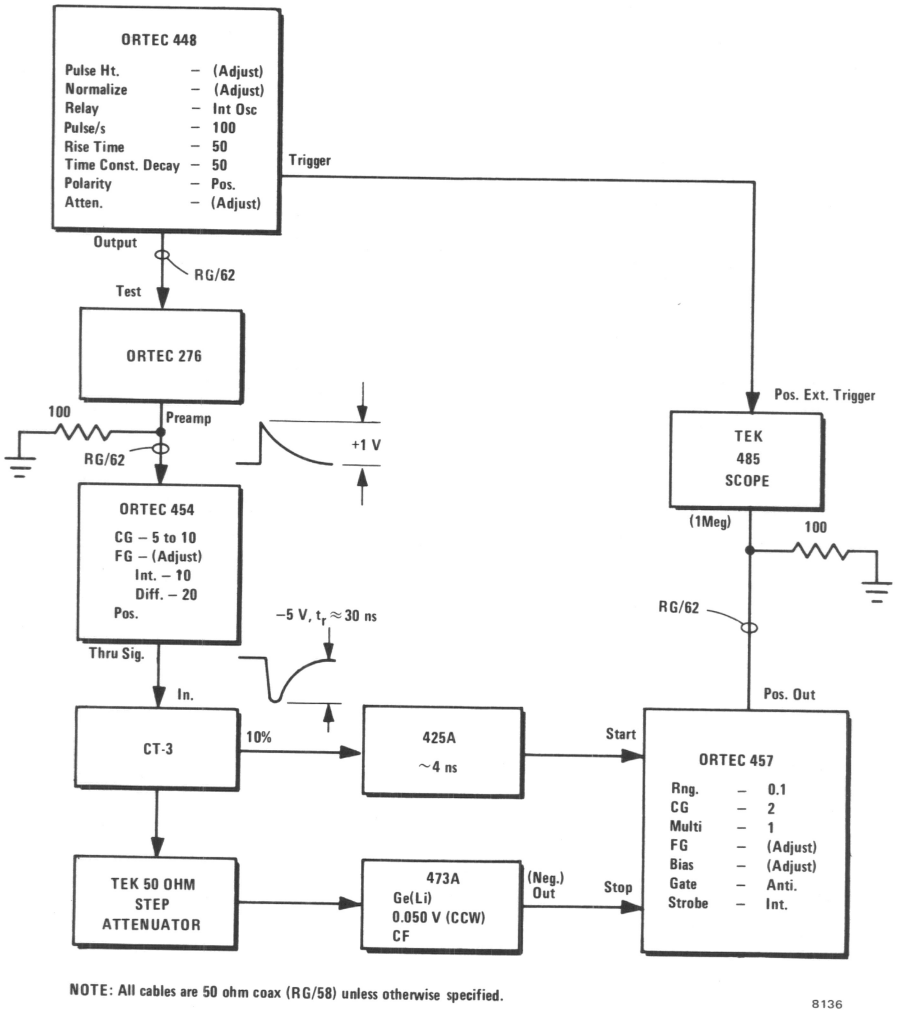


Fig. 7.4. Test Setup for Ge(Li) Mode Walk Test.

7.7. FACTORY REPAIR

This instrument can be returned to the ORTEC factory for service and repair at a nominal cost. Our standard procedure for repair ensures that the same quality control and checkout are used that would be used for a new instrument. Always contact Customer Services at ORTEC, (615) 482-4411, before sending in an instrument for repair to obtain shipping instructions and so that the required Return Authorization Number can be assigned to the unit. This number should be written on the address label and on the package to ensure prompt attention when the shipment reaches the factory.

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TIMING WITH Ge(Li) DETECTORS

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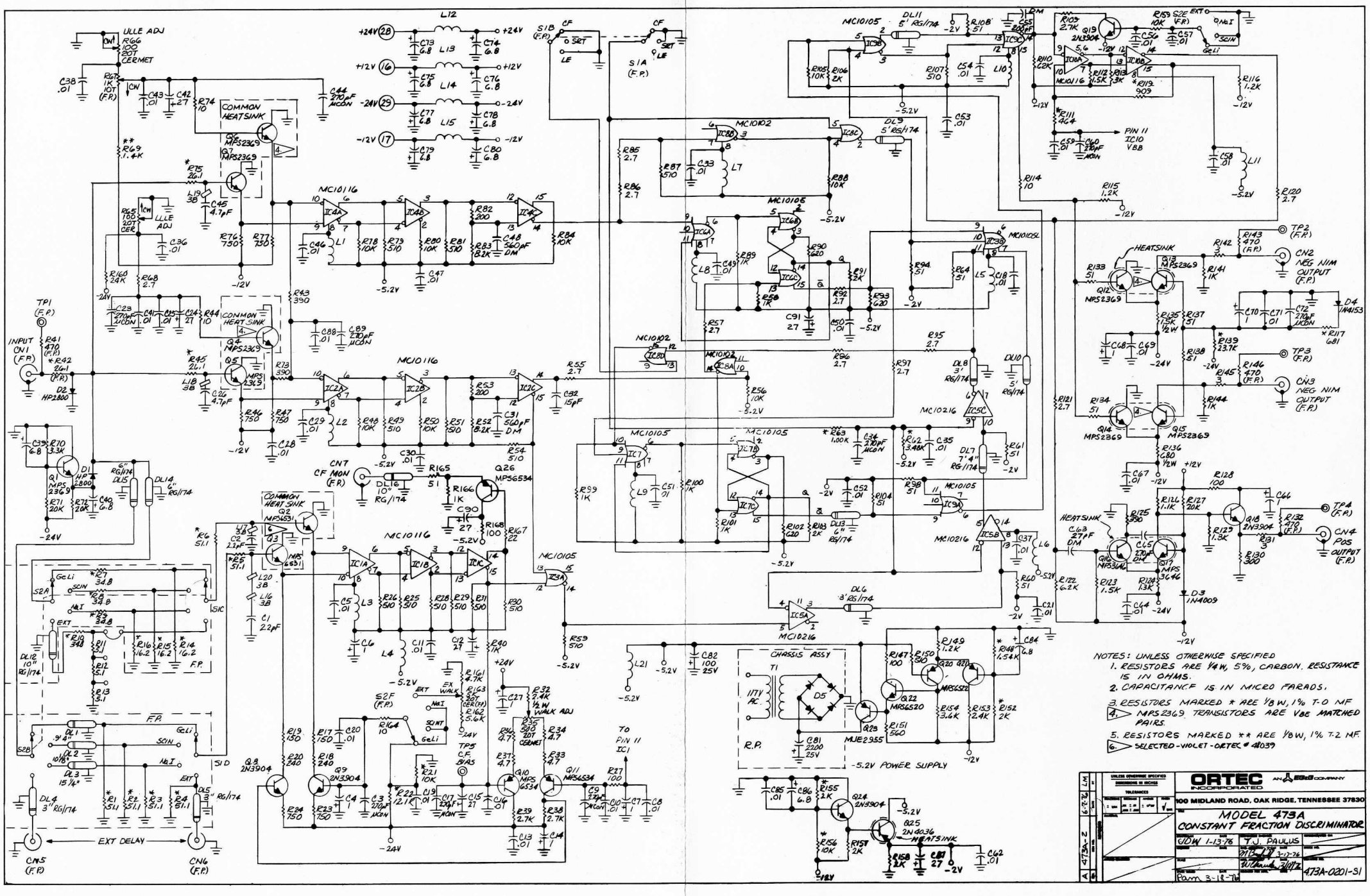
BIN/MODULE CONNECTOR PIN ASSIGNMENTS FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES PER TID-20893

Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	−3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	−24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Spare
*10	+6 volts	32	Spare
*11	−6 volts	*33	115 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Spare	**35	Reset (Scaler)
14	Spare	**36	Gate
15	Reserved	**37	Reset (Auxiliary)
*16	+12 volts	38	Coaxial
*17	−12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	115 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

Pins marked (*) are installed and wired in ORTEC 401A and 401B Modular System Bins.
Pins marked (*) and (**) are installed and wired in EG&G/ORTEC–HEP M250/N and M350/N NIMBINS.



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE ¼W, 5%, CARBON. RESISTANCE IS IN OHMS.
2. CAPACITANCE IS IN MICRO FARADS.
3. RESISTORS MARKED * ARE ⅛W, 1% T-0 MF
4. MPS2369 TRANSISTORS ARE Vbe MATCHED PAIRS.
5. RESISTORS MARKED ** ARE ⅛W, 1% T-2 MF.
6. SELECTED - VIOLET - ORTEC # A1039

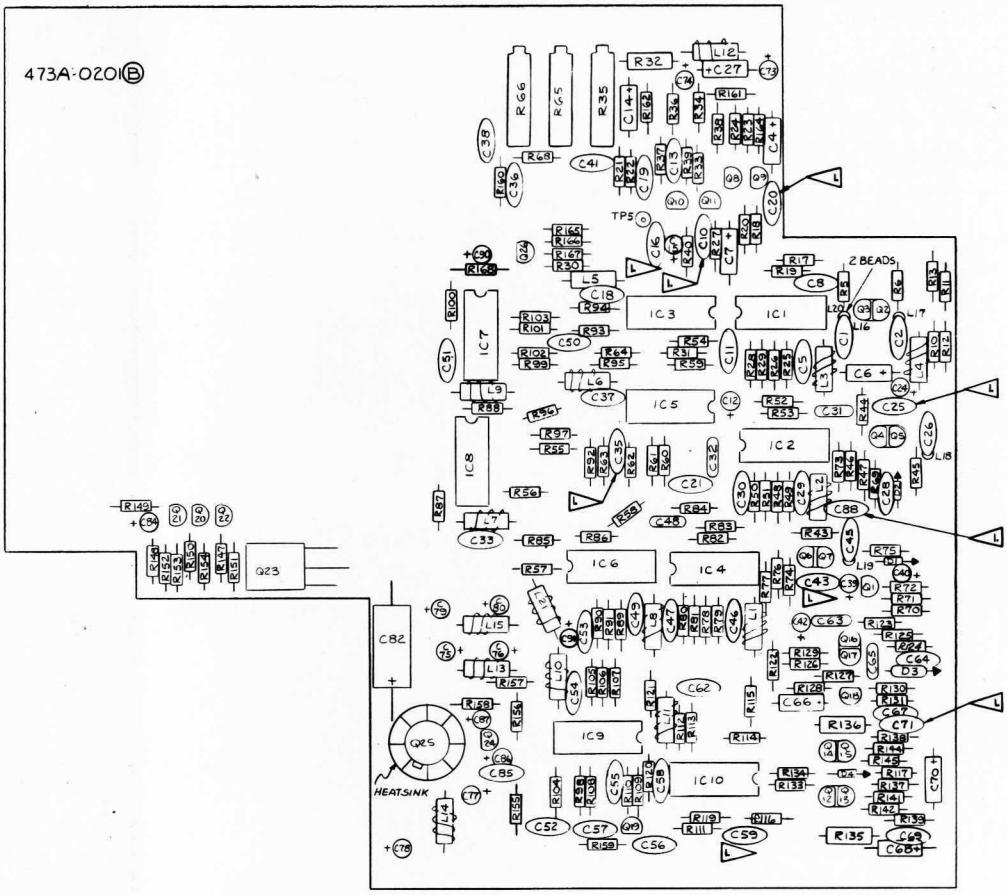
ORTEC INCORPORATED — AN EG&G COMPANY

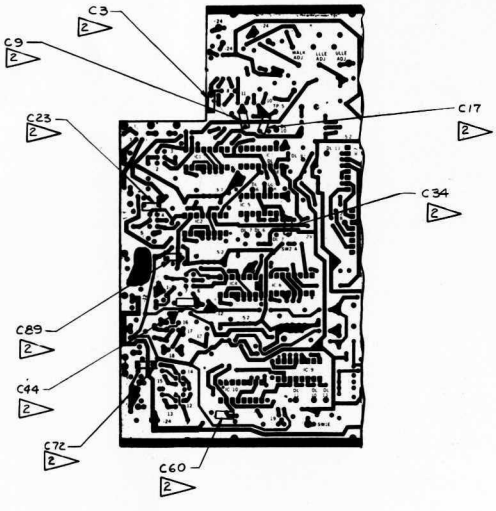
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

MODEL 473A
CONSTANT FRACTION DISCRIMINATOR

UDW 1-13-76 — TJ PAULUS — 3-12-76 — 473A-0201-S1

473A-Z — 6-7-76 LM — A

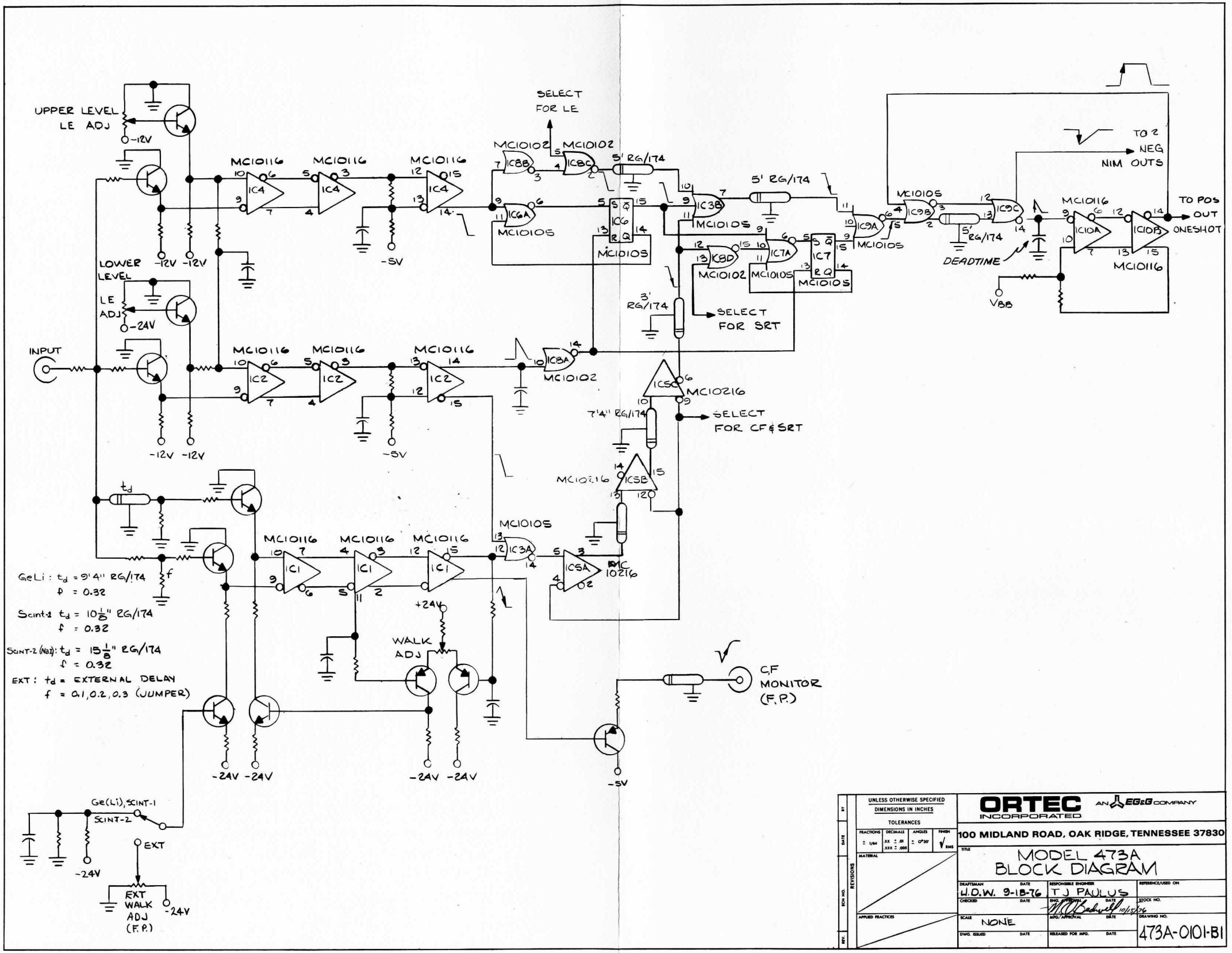




PARTIAL REAR VIEW

NOTES:

1. PIN CAPACITOR LEAD HOLES PRIOR TO WAVE SOLDERING.
2. FORM CAPACITOR LEADS ON CIRCUIT SIDE OF BOARD. INSTALL STRIPLINE CAPACITORS TO NEAREST POINT, WHERE LEAD PROTRUDES THROUGH BOARD, AFTER WAVE SOLDERING. CLIP EXCESS LEAD.



UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
FRACTIONS ± 1/64 | DECIMALS XX ± .01, XXX ± .005 | ANGLES ± 0°30' | FINISH √ RMS
MATERIAL
APPLIED PRACTICES
REVISIONS | BY | DATE | ECN NO.

ORTEC INCORPORATED — AN EG&G COMPANY

100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

TITLE: MODEL 473A BLOCK DIAGRAM

DRAFTSMAN H.D.W. 9-18-76	RESPONSIBLE ENGINEER T J PAULUS	REFERENCE/USED ON	
CHECKED	ENG. APPROVAL 10/15/76	STOCK NO.	
SCALE NONE	MFG. APPROVAL	DRAWING NO.	473A-0101-B1
DWG. ISSUED	RELEASED FOR MFG.		

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